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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,972	01/13/2004	Shaoher X. Pan	23340-08600	3780

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EXAMINER	
MARTINEZ, JOSEPH P	
ART UNIT	**PAPER NUMBER**
2873	

DATE MAILED: 05/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/756,972	PAN ET AL.	
	Examiner	Art Unit	
	Joseph P. Martinez	2873	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 13 January 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2-23-04, 3-22-04, 5-26-04, 6-28-04, 8-6-04, 4-1-05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 5, 7, 10, 12 and 14-17 are rejected under 35 U.S.C. 102(e) as being fully anticipated by Garverick et al. (6543286).

Re claim 1, Garverick et al. teaches for example, a spatial light modulator for use in a video display comprising: a control circuitry substrate (lower substrate 130, fig. 2) including: a plurality of electrodes (electrodes 120, fig. 2) for receiving selected voltages (voltages V_A and V_B, fig. 2); a memory buffer (content addressable memory (CAM) register buffer amplifier 244, fig. 8), a video display controller (control system, fig. 3) for

processing video signals (col. 3, ln. 2-3 and col. 16, ln. 55-58); and a pulse width modulation array (pulse width modulated voltage driving signals, fig. 4); and a mirror array substrate (MEMS region 132, fig. 2) bonded to the control circuitry substrate (figs. 1 and 2, col. 1, ln. 34-37, col. 2, ln. 39-43), the mirror array substrate including: an array of video display pixels (fig. 1, col. 3, ln. 2-3 and col. 16, ln. 55-58) comprising a plurality of micro mirror plates (mirror 116, fig. 1), a spacer support frame (support structure 112, fig. 2) for spacing the plurality of micro mirror plates apart from the control circuitry substrate (lower substrate 130, fig. 2) and supporting the micro mirror plates, and a plurality of hinges (torsion beams 114 and 118, fig. 1), each hinge connected to the spacer support frame and to a micro mirror plate, for allowing the micro mirror plate to rotate relative to the spacer support frame about an axis defined by the hinge (col. 1, ln. 38-45).

Re claim 7, Garverick et al. teaches for example, a spatial light modulator for use in a video display comprising: a control circuitry substrate (lower substrate 130, fig. 2) including: an electrode layer with a plurality of electrodes (electrodes 120, fig. 2) for receiving selected voltages (voltages V_A and V_B, fig. 2); and a control circuitry substrate including line memory buffers (content addressable memory (CAM) register buffer amplifier 244, fig. 8) and a pulse width modulation array (pulse width modulated voltage driving signals, fig. 4); and a mirror array substrate (MEMS region 132, fig. 2) bonded to the control circuitry substrate (figs. 1 and 2, col. 1, ln. 34-37, col. 2, ln. 39-43), the mirror

array substrate including an array of video pixel elements (fig. 1, col. 3, ln. 2-3 and col. 16, ln. 55-58) comprising a plurality of micro mirrors (mirror 116, fig. 1).

Re claim 17, Garverick et al. teaches for example, a spatial light modulator for use in a video display having both a micro mirror array and control circuitry integrated on one chip for improved data transfer rates, comprising: a micro mirror array substrate including: a plurality of micro mirror plates (mirror 116, fig. 1); a video pixel array (fig. 1, col. 3, ln. 2-3 and col. 16, ln. 55-58) comprising a plurality of micro mirrors (mirror 116, fig. 1); a spacer support frame (support structure 112, fig. 2) for spacing the plurality of micro mirror plates apart from the control circuitry substrate (lower substrate 130, fig. 2) and supporting the micro mirror plates; a plurality of hinges (torsion beams 114 and 118, fig. 1), each hinge connected to the spacer support frame and to a micro mirror plate, for allowing the micro mirror plate to rotate relative to the spacer support frame about an axis defined by the hinge (col. 1, ln. 38-45); and an electrode layer with a plurality of electrodes (electrodes 120, fig. 2) connected to the control circuitry for receiving selected voltages (voltages V_A and V_B, fig. 2) from the control circuitry and each electrode is associated with a micro mirror plate of the mirror array substrate so that the selected voltage received by an electrode creates an electric field that controls the rotation of the associated micro mirror plate and a direction at which light is reflected from the associated micro mirror plate (col. 1, ln. 38-45, wherein the office interprets controlling the mirror plate to include controlling the direction at which light is reflected); and wherein the control circuitry and the electrodes of the control circuitry substrate are

fabricated and then the control circuitry substrate is bonded to the mirror array substrate (figs. 1 and 2, col. 1, ln. 34-37, col. 2, ln. 34-54).

Re claim 2, Garverick et al. further teaches for example, a plurality of CMOS inverters, wherein each of the plurality of electrodes is driven by a different CMOS inverter (col. 10, ln. 12-16).

Re claims 5 and 12, Garverick et al. further teaches for example, the mirror array substrate is aligned with the control circuitry substrate so that each electrode is located under a micro mirror plate and associated with that micro mirror plate such that the selected voltage received by the electrode controls a rotational movement of the micro mirror plate (fig. 2, col. 1, ln. 38-45).

Re claim 10, Garverick et al. further teaches for example, a plurality of micro mirror plates (mirror 116, fig. 1), a spacer support frame (support structure 112, fig. 2) for spacing the plurality of micro mirror plates apart from the control circuitry substrate (lower substrate 130, fig. 2) and supporting the micro mirror plates, and a plurality of hinges (torsion beams 114 and 118, fig. 1), each hinge connected to the spacer support frame and to a micro mirror plate, for allowing the micro mirror plate to rotate relative to the spacer support frame about an axis defined by the hinge (col. 1, ln. 38-45).

Re claim 14, Garverick et al. further teaches for example, the plurality of electrodes (electrodes 120, fig. 2) of the control circuitry substrate are on a passivation layer (insulating oxide layer134, fig. 2).

Re claims 15 and 16, Garverick et al. further teaches for example, the passivation layer is on a circuitry layer that includes the line memory buffers (content addressable memory (CAM) register buffer amplifier 244, fig. 8, col. 2, ln. 39-43) and the pulse width modulation array (pulse width modulated voltage driving signals, fig. 4, col. 2, ln. 39-43) and the circuitry layer further includes a video display controller (control system, fig. 3, col. 2, ln. 39-43) adapted to process video signals (col. 3, ln. 2-3 and col. 16, ln. 55-58).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 3, 4, 8, 9, 11 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garverick et al. (6543286) as applied to claims 1, 7, 10 and 17 in view of Wu et al. (6542653).

Re claims 3 and 4, supra claim 1; re claims 8 and 9, supra claim 7; re claim 11, supra claim 10; and re claim 18, supra claim 17. Furthermore, Garverick et al. teaches the use of a micro mirror (mirror 116, fig. 1).

But, Garverick et al. fails to explicitly teach the micro mirror plates, the spacer support frame, and each of the plurality of hinges are part of a single continuous piece of material, wherein the material is single crystal silicon.

However, within the same field of endeavor, Wu et al. teaches for example, a spatial light modulator (micromachined structure 100, fig. 1) with control circuitry (controller 99, fig. 1) wherein the spacer support frame, and each of the plurality of hinges are part of a single continuous piece of material, wherein the material is single crystal silicon (fig. 1, col. 3, ln. 63-67 to col. 4, ln. 1-11).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the spatial light modulator of Garverick et al. with the micro mirror array made of single continuous piece of material, wherein the material is single crystal silicon because it provides mechanical advantages such as superior stiffness, durability, fatigue and deformation characteristics.

2. Claims 6, 13, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garverick et al. (6543286) as applied to claims 1, 7 and 17 in view of Patel et al. (US20020132389).

Re claims 6, 13 and 20, supra claims 1, 7 and 17, respectively. Furthermore, Garverick et al. teaches for example, bonding the control circuitry and micro mirror array (figs. 1 and 2, col. 1, ln. 34-37, col. 2, ln. 34-54).

But, Garverick et al. fails to explicitly teach the mirror array substrate is bonded with the control circuitry substrate by a low temperature bonding method performed at less than approximately 500 degrees Celsius.

However, within the same field of endeavor, Patel et al. teaches for example bonding an MEM device to control circuitry (para. 0007), including micro mirror arrays (para. 0002), by using various bonding methods including thermally cured epoxies (para. 0053).

But Patel et al. fails to explicitly teach the bonding method is performed at less than approximately 500 degrees Celsius.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform a bonding method at less than approximately 500 degrees Celsius, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the bonding process of Garverick et al. with the thermal bonding process of Patel et al. in order to precisely align the wafers.

Re claim 19, supra claim 17. Furthermore, Garverick et al. teaches for example, bonding the control circuitry and micro mirror array (figs. 1 and 2, col. 1, ln. 34-37, col. 2, ln. 34-54).

But, Garverick et al. fails to explicitly teach the micro mirror army is partially fabricated, then bonded to the control circuitry substrate, and then fabrication of the micro mirror array is completed.

However, within the same field of endeavor, Patel et al. teaches for example, teach the micro mirror army is partially fabricated, then bonded to the control circuitry substrate, and then fabrication of the micro mirror array is completed (para. 0007).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify fabrication process of Garverick et al. with the fabrication process of Patel et al. in order increase fabrication output.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph P. Martinez whose telephone number is 571-272-2335. The examiner can normally be reached on M-F 7:00 AM to 3:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Y. Epps can be reached on 571-272-2328. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
5-23-05

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